Digital Gate Driver IC with Real-Time Gate Current Change by Sensing Drain Current to Cope with Operating Condition Variations of SiC MOSFET

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***Abstract*-- A digital gate driver IC with real-time gate current (I_G) change by sensing drain current (I_D) is applied to SiC MOSFETs, and it is demonstrated that the IC always reduces switching loss and switching noise by always performing appropriate active gate driving even when the operating conditions of SiC MOSFETs, such as load current and junction temperature, change. The IC integrates all of a current-source based digital gate driver which changes I_G in 6 bits, a dI_D/dt sensor to detect I_G switching timing, and a controller into a single chip. In the turn-on measurement of an SiC MOSFET at 600 V and 25 ˚C, when the load current changes to 20 A, 70 A, and 120 A, compared with the conventional single-step gate drive, the active gate drive using the developed IC reduced the switching loss by 17 %, 12 %, and 11 % under I_D overshoot-aligned condition, respectively.**

***Index Terms*-- Gate driver, switching loss, switching noise, SiC.**

I. Introduction

A lot of active gate drivers (AGDs), where the gate driving waveform is controlled during the turn-on/off transients, have been proposed to reduce both the switching loss (E_{LOSS}) and the switching noise of power devices. AGDs can be classified into two types, open-loop control [1-6] and closed-loop control [7-20]. The closed-loop AGDs are required instead of the open-loop AGDs, because the optimal driving waveform changes depending on the operating conditions (e.g. load current (I_L) and junction temperature (T_J)) [21]. Fig. 1 summarizes the design choices in conventional closed-loop AGDs. To make the closed-loop AGDs practical, the following three points are required: (1) single-chip integration instead of PCB implementation for lower cost, (2) real-time control instead of iterative control to reliably handle dynamic change of operating conditions, and (3) programmable AGDs instead of fixed-function AGDs that require individual optimization for different product varieties of power devices. In the closed-loop AGDs, however, no previous paper has realized all of (1) to (3).

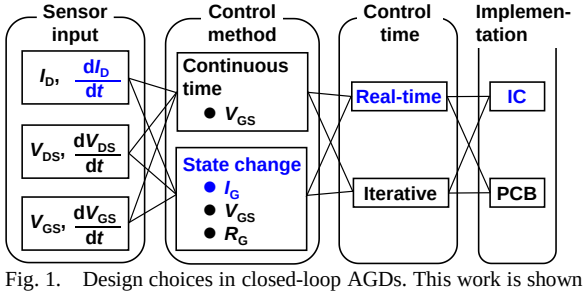

Fig. 1. Design choices in closed-loop AGDs. This work is shown in blue.

To solve the problems, a digital gate driver (DGD) IC with real-time gate current change (RGC) by sensing drain current (I_D) that realizes all of (1) to (3) was proposed in [22]. The design choices in [22] are shown in blue in Fig. 1. The IC [22] integrates all of a current-source based digital gate driver which changes gate current (I_G) in 6 bits, a dI_D/dt sensor to detect I_G switching timing, and a controller into a single chip. In [22], the operation was demonstrated for IGBTs. In contrast, in this paper, the DGD IC with RGC [22] is applied to SiC MOSFETs for the first time. It is shown that the IC always reduces E_{LOSS} and switching noise by always performing appropriate active gate driving even when I_L and T_J of an SiC MOSFET change.

II. Digital Gate Driver IC With Real-Time Gate Current Change

Figs. 2 and 3 show a circuit schematic and a timing chart of the DGD IC with RGC [22], respectively. In the following, turn-on is discussed, whereas the exact same is true for turn-off. The IC includes dI_D/dt detector for the state change, controller for RGC, and a 6-bit current-source type digital gate driver with variable I_G in 64 levels, where $I_G = n_{PMOS} \times 48$ mA and n_{PMOS} is an integer from 0 to 63. At turn-on, an active gate driving is performed in three slots from t_1 to t_3 with different I_G of strong (n_1) - weak (n_2) -strong (n_3), and this driving method is defined as stop-and-go gate drive (SGGD) [23]. n_1 to n_3 are preset by a digital input (Scan In), while t_1 and t_2 are automatically determined by RGC by sensing I_D. An important feature of this IC is the full integration of t_1 and t_2 real-time automatic control functions on a single chip. The real-time control is completed only by the IC and the external FPGAs or MCUs are not required. The real-time control of t_1 and t_2 is done by detecting dI_D/dt by sensing the voltage (V_{sS}) of the parasitic inductance (L_{sS}) between Kelvin source and power source in Fig. 2, because $V_{sS} = -L_{sS}$ (dI_D/dt). Specifically, as shown in Fig. 3, the end timing of t_1 is determined by detecting the negative V_{sS} at the beginning of I_D flow using a comparator with the reference voltage of V_{REFL}, and the end timing of t_2 is determined by

detecting the positive V_{SS} at the timing immediately after I_D overshoots using a comparator with the reference voltage of V_{REFH}. Fig. 4 shows a die photo of DGD IC fabricated with 180-nm BCD process. The die size is 2.0 mm by 2.5 mm.

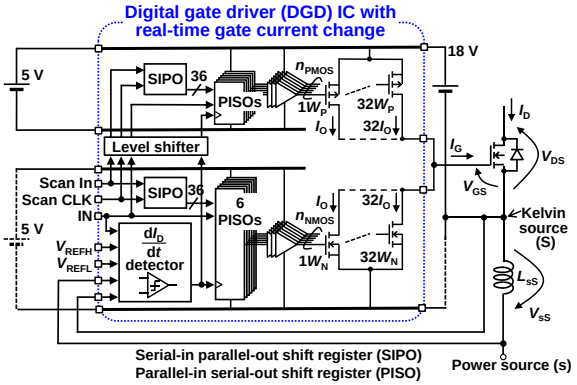

Fig. 2. Circuit schematic of digital gate driver (DGD) IC with real-time gate current change (RGC).

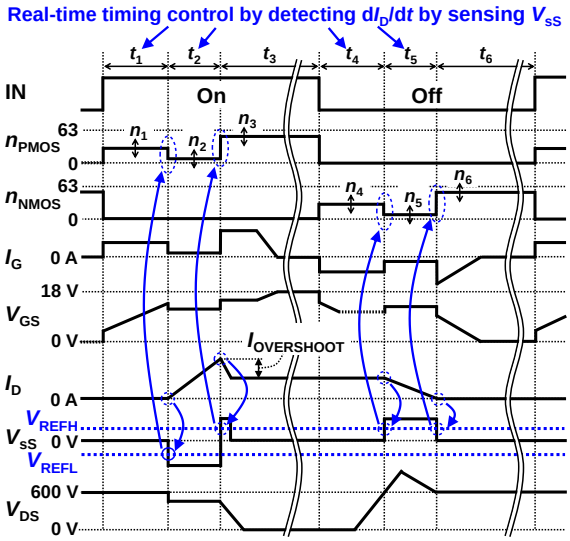

Fig. 3. Timing chart of DGD IC with RGC.

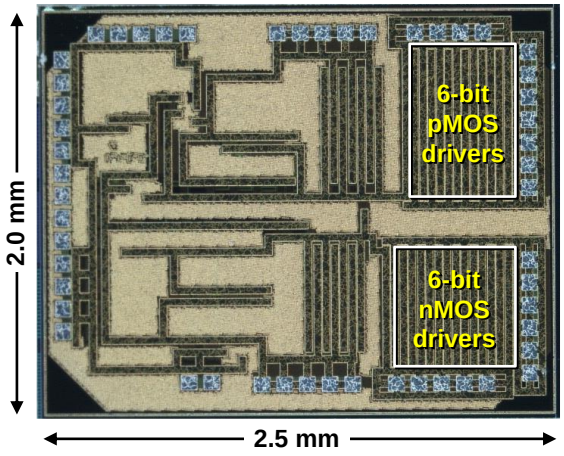

Fig. 4. Die photo of DGD IC fabricated with 180-nm BCD process.

III. Measured Results

A. Measurement Setup

Figs. 5 and 6 show a circuit schematic and a measurement setup of the double pulse test using the developed DGD IC and an SiC module (BSM120D12P2C005, 1200 V, 134 A), respectively. The SiC module is placed on a hotplate for measurement under different temperature. Figs. 7 (a) and (b) show timing charts of the conventional single-step gate drive (SSGD) and the proposed SGGD for comparison, respectively. In SSGD, n_1 is varied, which emulates a conventional gate driver with varied gate resistance. In SGGD, (n_1, n_2, n_3) are preset to (30, 13, 27), and t_1 and t_2 are automatically determined by RGC by sensing I_D.

The reason for setting (n_1, n_2, n_3) = (30, 13, 27) is explained here. In SGGD, in principle, n_1 should be set large to reduce turn-on delay, n_2 small to reduce the drain current overshoot ($I_{OVERSHOOT}$), and n_3 large to reduce

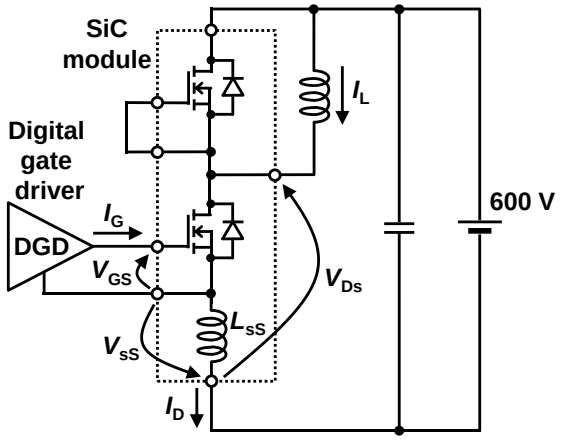

Fig. 5. Circuit schematic of double pulse test.

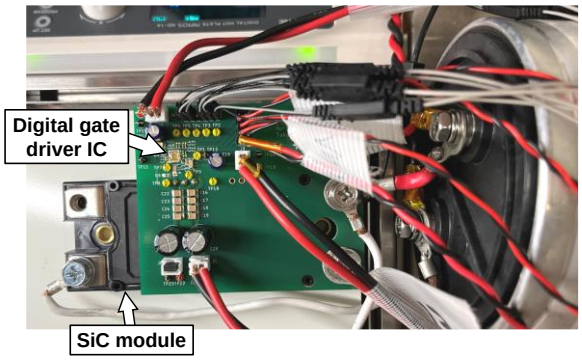

Fig. 6. Photo of measurement setup.

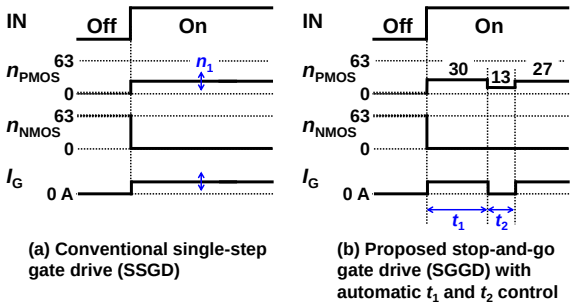

Fig. 7. Timing charts for turn-on.

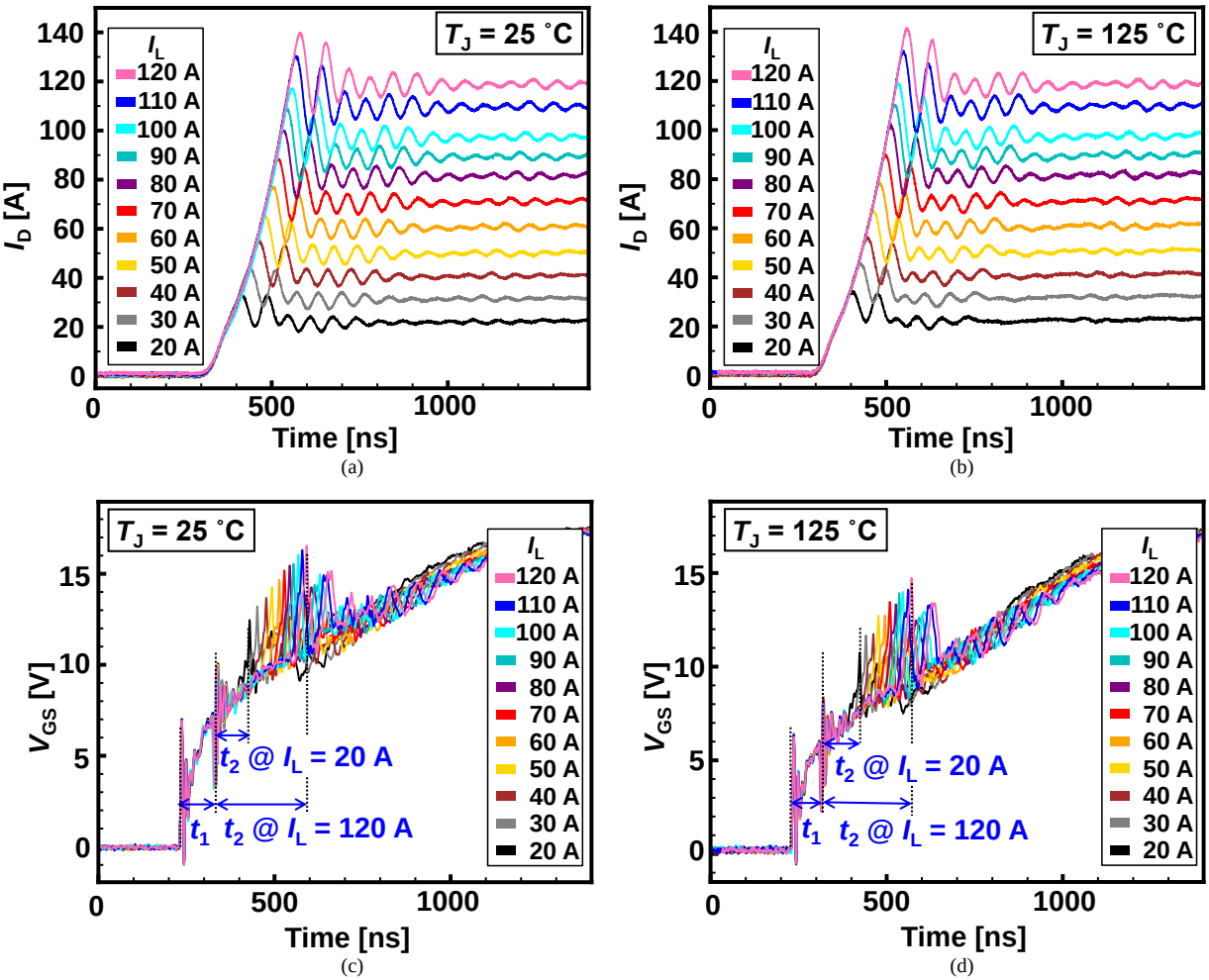

Fig. 8. Measured waveforms in SGGD with RGC with varied I_L from 20 A to 120 A in 10 A increments. (a) Measured I_D waveforms at T_J = 25 ˚C. (b) Measured I_D waveforms at T_J = 125 ˚C. (c) Measured V_{GS} waveforms at T_J = 25 ˚C. (d) Measured V_{GS} waveforms at T_J = 125 ˚C.

E_{LOSS} [23]. In the actual measurements, however, n_1 = 30, because if n_1 is set to 31 or higher, ringing at the beginning of the t_1 period of V_{SS} waveform shown later in Figs. 12 (b), 13 (b), and 14 (b) increases and exceeds V_{REFH} and V_{REFL}, causing the dI_D/dt detector to make a false detection. In addition, n_3 = 27 was set for the measurements, because if n_3 is set to 28 or higher, the second overshoot of I_D shown in Figs. 12 (b), 13 (b), and 14 (b) will be higher than the first overshoot of I_D, and $I_{OVERSHOOT}$ will not be controlled by n_2. Finally, n_2 is a parameter with a degree of freedom in its setting. In the pre-preparation measurements, it was confirmed that the proposed SGGD operates normally in the range of n_2 from 10 to 20. Setting n_2 = 10 results in a large E_{LOSS} and small $I_{OVERSHOOT}$, while setting n_2 = 20 results in a small E_{LOSS} and large $I_{OVERSHOOT}$. In this paper, n_2 = 13 was set to balance E_{LOSS} and $I_{OVERSHOOT}$.

B. Proposed SGGD at Various I_L and T_J

Figs. 8 (a) to (b) show the measured I_D waveforms and Figs. 8 (c) to (d) show the measured gate-source voltage (V_{GS}) waveforms in SGGD with RGC with varied I_L from 20 A to 120 A in 10 A increments at T_J of 25 ˚C and 125 ˚C, respectively. In Figs. 8 (c) and (d), the periods t_1 and t_2 can be estimated from the surges in V_{GS} waveforms. t_1 is independent of I_L, while t_2 is dependent on I_L. Fig. 9 shows the measured t_2 vs. I_L at T_J of 25 ˚C and 125 ˚C. It is clearly observed that as I_L increases, t_2 is automatically increased by RGC. On the other hand, the T_J dependence of t_2 is almost negligible. In contrast, the T_J dependence of t_2 was clearly observed for IGBTs [22]. The reason why the T_J dependence of t_2 is almost negligible for SiC MOSFETs can be explained by the smaller temperature dependence of the SiC device characteristics compared to IGBTs [24].

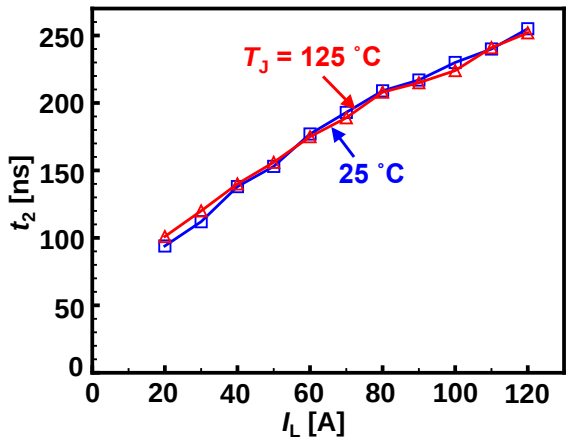

Fig. 9. Measured t_2 vs. I_L at T_J = 25 ˚C and 125 ˚C extracted from Figs. 8 (c) and (d).

C. Comparison of E_{LOSS} and $I_{OVERSHOOT}$ between Conventional SSGD and Proposed SGGD

Figs. 10 (a) to (c) show the measured E_{LOSS} vs. $I_{OVERSHOOT}$ of the conventional SSGD and the proposed SGGD at I_L = 20 A, 70 A, and 120 A, respectively. In each graph, T_J is varied to 25 ˚C and 125 ˚C. The blue curve, which represents T_J = 25 ˚C, and red curve, which represents T_J = 125˚C, show the trade-off curves of the conventional SSGD with varied n_1 from 5 to 63. In all cases, the proposed SGGD has lower E_{LOSS} and lower $I_{OVERSHOOT}$ than the conventional SSGD. At T_J = 25 ˚C, when I_L is varied to 20 A, 70 A, and 120 A, compared with the conventional SSGD, the proposed SGGD reduces E_{LOSS} by 17 %, 12 %, and 11 %, respectively, under the $I_{OVERSHOOT}$-aligned condition, while it reduces $I_{OVERSHOOT}$ by 17 %, 12 %, and 12 %, respectively, under the E_{LOSS}-aligned condition. At T_J = 125 ˚C, when I_L is varied to 20 A, 70 A, and 120 A, compared with the conventional SSGD, the proposed SGGD reduces E_{LOSS} by 21 %, 10 %, and 9 %, respectively, under the $I_{OVERSHOOT}$-aligned condition, while it reduces $I_{OVERSHOOT}$ by 18 %, 11 %, and 5 %, respectively, under the E_{LOSS}-aligned condition.

In Figs. 10 (a) and (c), Points A1 to A3, Points B1 to B3, and Points C1 to C3 are defined for (I_L, T_J) = (20 A, 25 ˚C), (120 A, 25 ˚C), and (120 A, 125 ˚C), respectively,

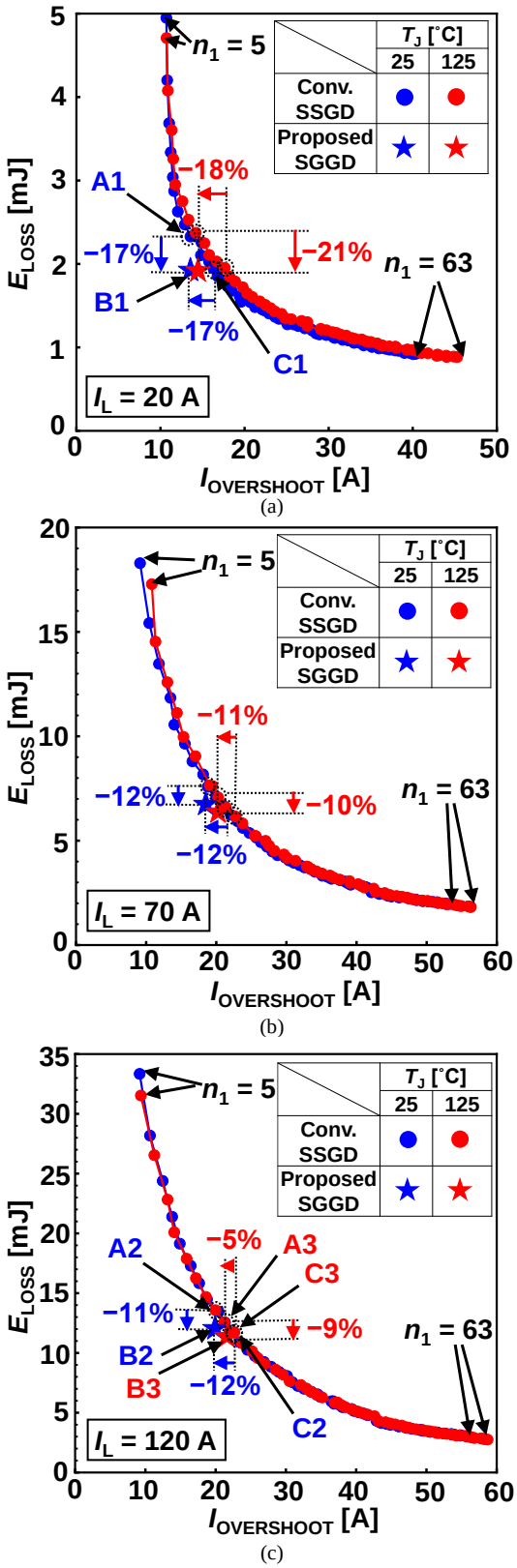

Fig. 10. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SSGD and proposed SGGD at T_J = 25 ˚C and 125 ˚C. (a) I_L = 20 A. (b) I_L = 70 A. (c) I_L = 120 A.

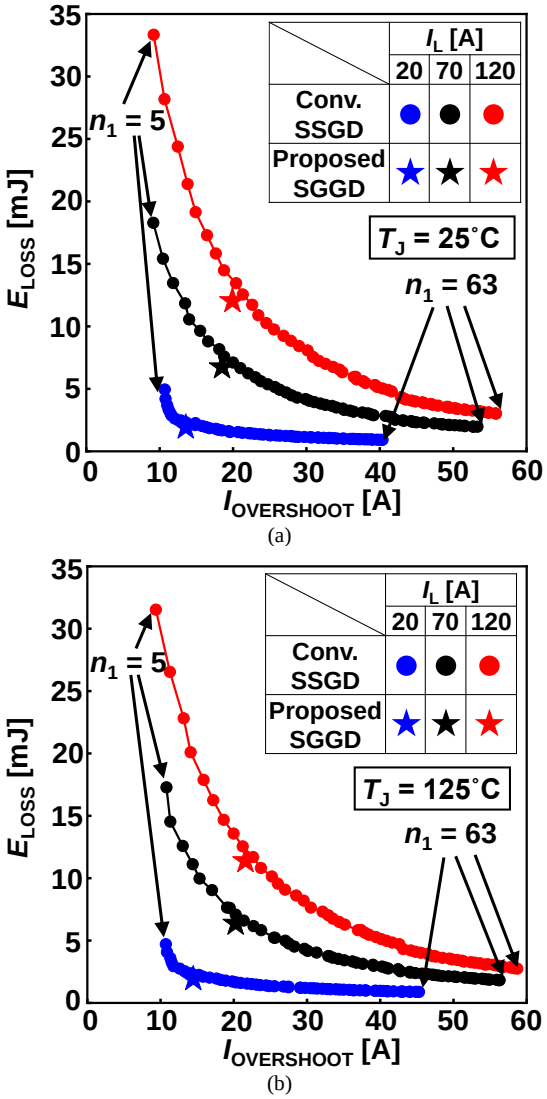

Fig. 11 Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SSGD and proposed SGGD at I_L = 20 A, 70 A, and 120 A. (a) T_J = 25 ˚C. (b) T_J = 125 ˚C.

where Points ”B”s are the proposed SGGD, Point “A”s are the conventional SSGD with closest $I_{OVERSHOOT}$ comparing to proposed ones, and Point “C”s are the conventional SSGD with the closest E_{LOSS} comparing to proposed ones. The measured waveforms for these nine points are shown later in Figs. 12 to 14.

Figs. 11 (a) and (b) show the measured E_{LOSS} vs. $I_{OVERSHOOT}$ of the conventional SSGD and the proposed SGGD at T_J = 25 ˚C and 125 ˚C, respectively. In each graph, I_L is varied to 20 A, 70 A, and 120 A. Similarly, in each graph, the red curve, which represents I_L = 120 A, black curve, which represents I_L = 70 A, and blue curve, which represents I_L = 20 A, show the trade-off curves of the conventional SSGD with varied n_1 from 5 to 63. The proposed SGGD has advantage over conventional SSGD on lower E_{LOSS} and lower $I_{OVERSHOOT}$.

Figs. 12 (a) to (c) show the measured waveforms of Point A1, which represents the waveform of SGGD with n_1 = 13, Point B1, the proposed SGGD, and Point C1, which represents the waveform of SGGD with n_1 = 17 in

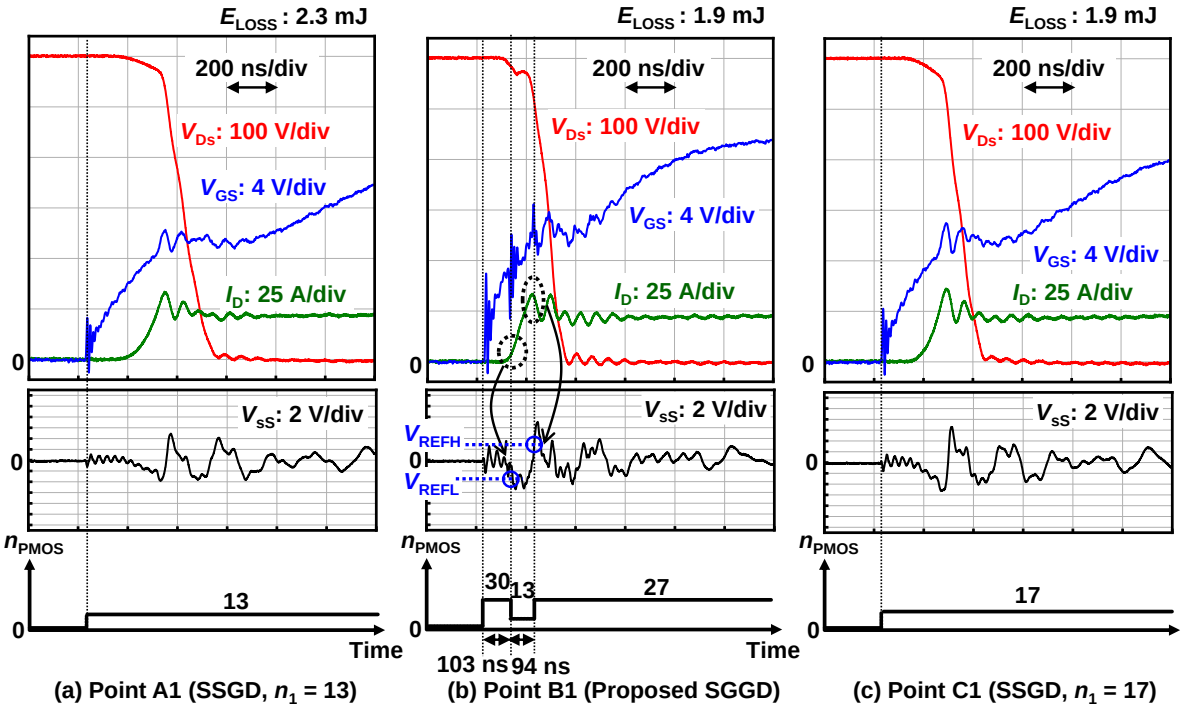

Fig. 12 Measured waveforms of Point A1, Point B1, and Point C1 in Fig. 10 (a) at I_L = 20 A and T_J = 25˚C.

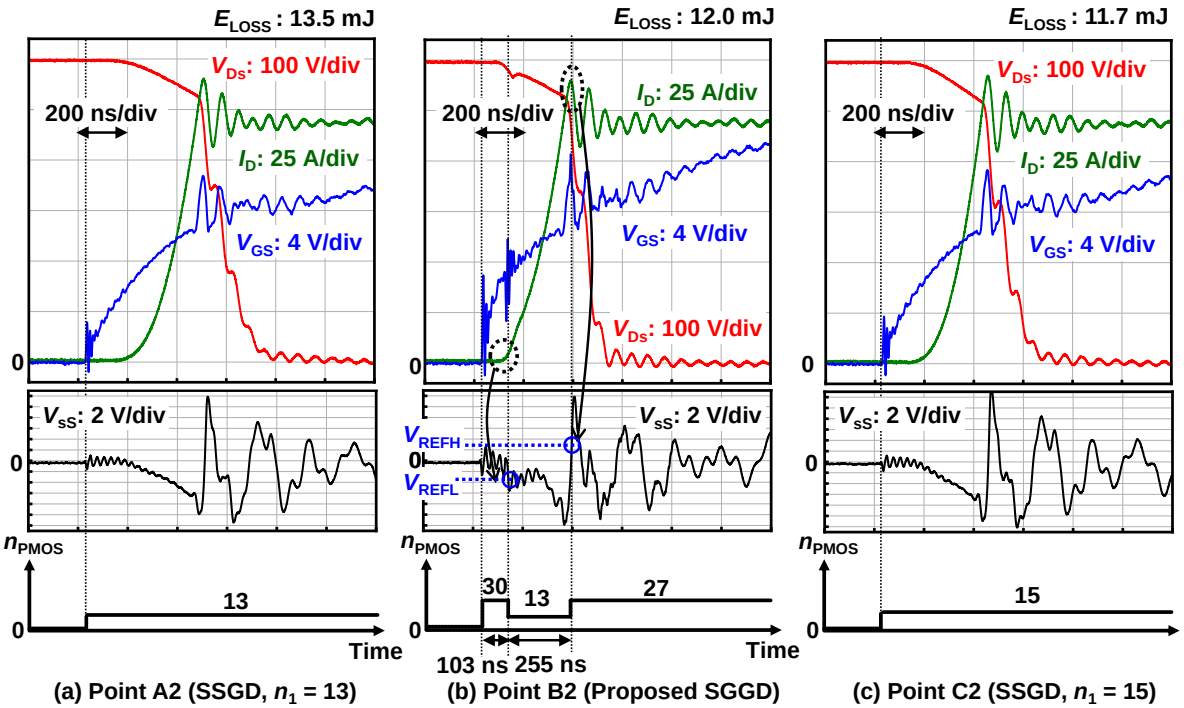

Fig. 13 Measured waveforms of Point A2, Point B2, and Point C2 in Fig. 10 (c) at I_L = 120 A and T_J = 25˚C.

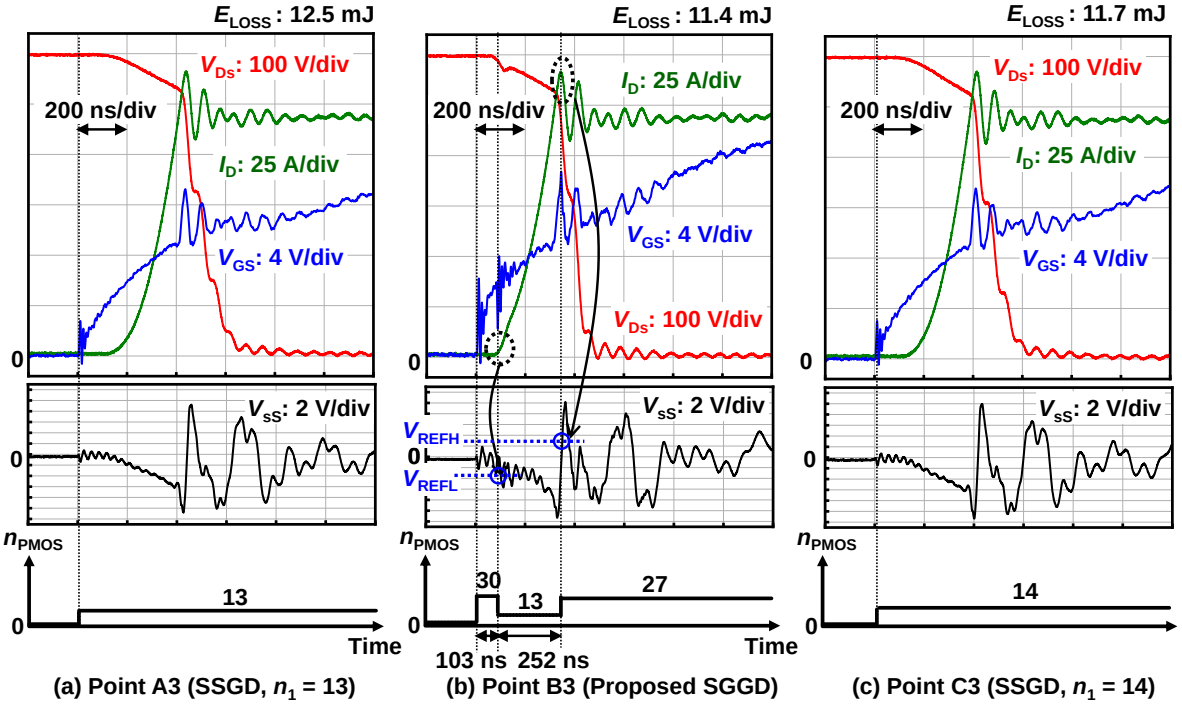

Fig. 14 Measured waveforms of Point A3, Point B3, and Point C3 in Fig. 10 (c) at I_L = 120 A and T_J = 125˚C.

Fig. 10 (a), respectively, under I_L = 20 A, T_J = 25˚C condition. Fig. 12 (b) clearly shows that the start of I_D flow and I_D overshoot are properly detected by comparing V_{SS} with V_{REFL} and V_{REFH}, and that SGGD is realized with t_1 and t_2 correctly controlled. Compared with the conventional SSGD (Point A1 and Point C1), the proposed SGGD (Point B1) reduces E_{LOSS} from 2.3 mJ to 1.9 mJ by 17 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 17 % under E_{LOSS}-aligned condition.

Figs. 13 (a) to (c) show the measured waveforms of Point A2, B2, and C2 in Fig. 10 (c), as SGGD with n_1 = 13, the proposed SGGD, and SGGD with n_1 = 15, respectively, under I_L = 120 A, T_J = 25˚C condition. Fig. 13 (b) clearly shows that the start of I_D flow and I_D overshoot are properly detected by V_{SS}. Note also that comparing t_2 in Fig. 12 (b) and Fig. 13 (b), where I_L changed from 20 A to 120 A, t_2 increased from 94 ns to 255 ns. The I_L dependence of t_2 is successfully controlled automatically by the proposed RGC. Compared with the conventional SSGD (Point A2 and Point C2), the proposed SGGD (Point B2) reduces E_{LOSS} from 13.5 mJ to 12.0 mJ by 11 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 12 % under E_{LOSS}-aligned condition.

Similarly, Figs. 14 (a) to (c) show the measured waveforms of Point A3, B3, and C3, as SGGD with n_1 = 13, the proposed SGGD, and SGGD with n_1 = 14, respectively, under I_L = 120 A, T_J = 125 ˚C condition. In Fig. 14 (b), automatic control of t_1 and t_2 has been successfully achieved by detecting V_{SS} comparing to V_{REFL} and V_{REFH}. Compared with the conventional SSGD (Point A3 and Point C3), the proposed SGGD (Point B3) reduces E_{LOSS} from 12.5 mJ to 11.4 mJ by 9 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 5 % under E_{LOSS}-aligned condition.

TABLE I
COMPARISON TABLE OF CLOSED-LOOP AGDS

	TPEL'15 [11]	TPEL'18 [12]	TPEL'21 [14]	ISSCC'19 [13]	ISSCC'21 [18]	This work
Target power device	IGBT	IGBT	SiC MOSFET	Si MOSFET	GaN FET	SiC MOSFET
Sensor input	dI_C/dt, V_{CE}	dI_C/dt, V_{CE}	dI_C/dt	V_{DS}	V_{DD} of high-side gate driver	dI_D/dt
Feedback control target	V_{GE} waveform	Timing of state change	Timing of state change	Timing of state change	Timing of state change	Timing of state change
Real-time control	Yes	Yes	Yes	No	No	Yes
Number of states per switching		4	3	3	3	3
Preset parameters for each state		I_G	V_{GS}	R_G	I_G	I_G
Levels of parameter		NA	2	2	3	6 bit
Implementation	PCB	PCB	PCB	IC (Not fully integrated)*	IC (Fully integrated)	IC (Fully integrated)
IC Process				130 nm HV CMOS	500 nm, 600 V SOI**	180 nm BCD

*Voltage divider for V_{DS} is not integrated.
**High-voltage IC process with the same breakdown voltage as V_{CC} of main circuit is required.

Table I shows a comparison table of the closed-loop AGDs. The DGD IC with RGC [22] used in this work was the first work achieving the fully integrated IC, the real-time control, and the programmable I_G in the closed-loop AGDs. In this paper, the DGD IC with RGC [22] is applied to SiC MOSFETs for the first time.

IV. CONCLUSIONS

The DGD IC with RGC [22], integrating all of the current-source based digital gate driver which changes I_G in 6 bits, a dI_D/dt sensor to detect I_G switching timing, and a controller into a single chip, is applied to SiC MOSFETs for the first time. The IC always reduces E_{LOSS} and $I_{OVERSHOOT}$ by the real-time control of t_1 and t_2 even when I_L and T_J of an SiC MOSFET change. In the turn-on measurement of an SiC MOSFET at 600 V and 25 ˚C, when I_L is varied to 20 A, 70 A, and 120 A, compared with

the conventional SSGD, the proposed SGGD reduces E_{LOSS} by 17 %, 12 %, and 11 %, respectively, under the $I_{OVERSHOOT}$-aligned condition, while it reduces $I_{OVERSHOOT}$ by 17 %, 12 %, and 12 %, respectively, under the E_{LOSS}-aligned condition.

ACKNOWLEDGMENT

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